

MULTIPROCESSOR SYSTEM AND METHOD FOR SIMULTANEOUSLY PLACING ALL PROCESSORS INTO DEBUG MODE

Abstract of the Disclosure

Multiple processors of a multiprocessor system are placed into a debug
5 mode of operation approximately simultaneously when one processor initially
enters the debug mode as a result of incurring a debug event. The other
processors enter the debug mode as a result of the one processor asserting a
debug event signal upon initially entering the debug mode. A logic circuit
associated with each processor responds to any debug event signal asserted by
10 another processor and the failure of its associated processor to assert a debug
event signal, to assert an external debug break signal to the associated processor
and place the associated processor into the debug mode.

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